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L7	L4 and (java near5 reflection\$1)	0
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PIPELINE FLOW CONTROL OPTIMIZATION SOFTWARE, AND **METHODS**

Inventor: FERBER PHILIP E (US); FOUTS KENNETH B

Applicant: FERBER PHILIP E (US); FOUTS KENNETH B (US); (+5)

(US); (+5)

EC:

IPC: G05D7/00; G05D7/00

Publication info: WO2006014372 - 2006-02-09

2 Pipeline flow control optimization software and methods

Inventor: FERBER E P (US); FOUTS B K (US); (+5)

Applicant:

FC: G05D7/06F4B2

IPC: G05D7/00; G05D7/00

Publication info: US2006009881 - 2006-01-12

SYSTEM TO FACILITATE PIPELINE MANAGEMENT, SOFTWARE, AND RELATED METHODS

Inventor: TARABZOUNI THAMER K (SA); AL-MEJNA

ABDULAZIZ K (SA); (+1)

Applicant: SAUDI ARABIAN OIL CO (SA); ARAMCO

SERVICES COMPANY (US); (+3)

IPC: G06F12/00; G06F; G06F12/00 (+1)

Publication info: WO2005017703 - 2005-02-24

Software-implemented transform and lighting module and pipeline for graphics rendering on embedded platforms using a fixed-point normalized homogenous coordinate system

Inventor: WANG LIFENG (CN); DENG KE (CN); (+2)

Applicant: MICROSOFT CORP (US)

IPC: G06F17/00; G06F17/00; (IPC1-7): G06F17/00

Publication info: US2005091616 - 2005-04-28

Apparatus and method for improved execution of a software pipeline loop procedure in a digital signal processor

Inventor: ANDERSON TIMOTHY (US); ASAL MICHAEL D Applicant:

(US); (+1)

EC: G06F9/32B6; G06F9/38E

IPC: G06F9/45; G06F15/00; G06F9/45 (+3)

Publication info: US2003154469 - 2003-08-14

Apparatus and method for resolving an instruction conflict in a software pipeline nested loop procedure in a digital signal processor

Inventor: ASAL MICHAEL D (US); STOTZER ERIC J

Applicant:

EC: G06F9/32B6; G06F9/38E; (+1)

IPC: G06F9/32; G06F9/38; G06F9/32 (+2)

Publication info: US2003182511 - 2003-09-25

Apparatus and method for a software pipeline loop procedure in a digital signal processor

Inventor: STOTZER ERIC J (US); KRUEGER STEVEN D Applicant:

(US); (+1)

EC: G06F9/32B6; G06F9/38E; (+1)

IPC: G06F9/32; G06F9/38; G06F9/32 (+2)

Publication info: US2003120900 - 2003-06-26

Apparatus and method for executing a nested loop program with a software pipeline loop procedure in a digital signal processor

Inventor: STOTZER ERIC J (US); ASAL MICHAEL D

Applicant:

(US)

EC: G06F9/32B6

IPC: G06F9/00; G06F9/00; (IPC1-7): G06F9/00

Publication info: US2003120905 - 2003-06-26

Apparatus and method for processing an interrupt in a software pipeline loop procedure in a digital signal processor

Inventor: STOTZER ERIC J (US); KRUEGER STEVE D

(US); (+2)

EC:

IPC: G06F9/00; G06F9/00; (IPC1-7): G06F9/00

Publication info: US2003120899 - 2003-06-26

10 Apparatus and method for exiting from a software pipeline loop procedure in a digital signal processor

Inventor: GRANSTON ELANA D (US); STOTZER ERIC J Applicant:

(US); (+2)

EC: G06F9/32B6; G06F9/38E; (+1)

IPC: G06F9/32; G06F9/38; G06F9/32 (+2)

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11 SOFTWARE SIMULATOR FOR PIPELINE TYPE PROCESSOR

Inventor: TANAKA NOBUYUKI; TOMITA NORIYUKI;

Applicant: SANYO ELECTRIC CO

(+1)

EC:

IPC: G06F9/38; G06F11/28; G06F9/38 (+3)

Publication info: JP2000276376 - 2000-10-06

12 Method for parallelizing software graphics geometry pipeline rendering

Inventor: KWOK THOMAS YU-KIU (US);

Applicant: IBM (US)

NARAYANASWAMI CHANDRASEKHAR (US); (+1)

EC: G06F9/46A; G06F9/46C4

IPC: G06F9/48; G06F9/50; G06F9/46 (+1)

Publication info: US6088044 - 2000-07-11

NON-INVASION SOFTWARE BREAK POINT IN PROCESSOR

INSTRUCTION EXECUTION PIPELINE

Inventor: DEAO DOUGLAS E; SESHAN NATARAJAN

Applicant: TEXAS INSTRUMENTS INC

EC: G06F9/30Z; G06F9/318; (+3)

IPC: G06F9/30; G06F9/318; G06F9/38 (+13)

Publication info: JP10326189 - 1998-12-08

Non-intrusive software breakpoints in a processor instruction execution pipeline

Inventor: DEAO DOUGLAS E (US); SESHAN NATARAJAN Applicant: TEXAS INSTRUMENTS INC (US)

(US)

EC: G06F9/318; G06F9/38P; (+1)

IPC: G06F9/318; G06F9/38; G06F11/36 (+4)

IPC: G06F9/38; G06F9/38; (IPC1-7): G06F9/38

Publication info: US6016555 - 2000-01-18

SOFTWARE BRANCHING SYSTEM IN PIPELINE MACHINE

Inventor: TAKEMURA EIJI

Applicant: NEC SOFTWARE LTD

FC: Publication info: JP6059889 - 1994-03-04

METHOD OF MINIMIZING INTERRUPTION OF PIPELINE TREATMENT OF HARDWARE BY USING SOFTWARE-SCHEDULING TECHNIQUE

DURING COMPILE

Inventor: SUTEIIBUN II KINGU

Applicant: BULL HN INFORMATION SYST

EC: G06F9/45E5

IPC: G06F9/38; G06F9/45; G06F9/38 (+3)

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